CLAIMS

1. A finger front end for processing a plurality of channels, comprising:

a shift register for receiving and shifting in I and Q samples, wherein a plurality of the I and Q samples are accessible in parallel fashion;

a parallel sum calculator for receiving the plurality of I and Q samples and producing an I and Q result; and

a scheduler for controlling the shift register and the parallel sum calculator such that they are time-shared to produce results in sequence for each of the plurality of channels.

2. A receiver having a finger front end for processing a plurality of channels comprising:

a shift register for receiving and shifting in I and Q samples, wherein a plurality of the I and Q samples are accessible in parallel fashion;

a parallel sum calculator for receiving the plurality of I and Q samples and producing an I and Q result; and

a scheduler for controlling the shift register and the parallel sum calculator such that they are time-shared to produce results in sequence for each of a plurality of channels.

3. The receiver of claim 2, further comprising a digital signal processor for configuring each of the plurality of channels and receiving their corresponding outputs.

4. The receiver of claim 3, further comprising a searcher for determining channel parameters and providing them to the digital signal processor for configuration of each of the plurality of channels therewith.

5. An access terminal for use in a CDMA system including a receiver for processing a plurality of channels, comprising:

a shift register for receiving and shifting in I and Q samples, wherein a plurality of the I and Q samples are accessible in parallel fashion;

a parallel sum calculator for receiving the plurality of I and Q samples and producing an I and Q result; and

a scheduler for controlling the shift register and the parallel sum calculator such that they are time-shared to produce results in sequence for each of a plurality of channels.

6. An access point for use in a CDMA system including a receiver for processing a plurality of channels, comprising:

a shift register for receiving and shifting in I and Q samples, wherein a plurality of the I and Q samples are accessible in parallel fashion;

a parallel sum calculator for receiving the plurality of I and Q samples and producing an I and Q result; and

a scheduler for controlling the shift register and the parallel sum calculator such that they are time-shared to produce results in sequence for each of a plurality of channels.

7. A CDMA2000 system including a receiver for processing a plurality of channels comprising:

a shift register for receiving and shifting in I and Q samples, wherein a plurality of the I and Q samples are accessible in parallel fashion;

a parallel sum calculator for receiving the plurality of I and Q samples and producing an I and Q result; and

a scheduler for controlling the shift register and the parallel sum calculator such that they are time-shared to produce results in sequence for each of a plurality of channels.

8. A W-CDMA system including a receiver for processing a plurality of channels, comprising:

a shift register for receiving and shifting in I and Q samples, wherein a plurality of the I and Q samples are accessible in parallel fashion;

a parallel sum calculator for receiving the plurality of I and Q samples and producing an I and Q result; and

a scheduler for controlling the shift register and the parallel sum calculator such that they are time-shared to produce results in sequence for each of a plurality of channels.

9. An HDR system including a receiver for processing a plurality of channels, comprising:

a shift register for receiving and shifting in I and Q samples, wherein a plurality of the I and Q samples are accessible in parallel fashion;

a parallel sum calculator for receiving the plurality of I and Q samples and producing an I and Q result; and

a scheduler for controlling the shift register and the parallel sum calculator such that they are time-shared to produce results in sequence for each of a plurality of channels.

10. In a finger front end, a method of performing chip rate processing for a plurality of channels, comprising:

receiving I and Q samples as inputs to a shift register sized to hold a quantity of I and Q samples sufficient for a round;

accessing a plurality of I and Q samples spaced chip widths apart simultaneously from the shift register in accordance with an index address, the index address corresponding to I and Q samples associated with a channel; and

performing a parallel sum calculation on the plurality of I and Q samples to produce an I and Q result, the accessing and parallel sum calculation being performed once per round for each of a plurality of channels.

11. The method of claim 10, wherein the parallel sum calculation comprises:

generating a plurality of I and Q PN sequence values each cycle according to the channel;

despreading the plurality of I and Q samples with the plurality of I and Q PN sequence values to produce a plurality of despread I and Q results; and

summing the plurality of despread I and Q results to produce the I and Q result.

12. In a finger front end, a method of performing chip rate processing for a plurality of channels, comprising:

receiving I and Q samples as inputs to a shift register at a sampling rate, the shift register sized to hold a quantity of I and Q samples sufficient for a round;

accessing a plurality of I and Q samples spaced chip widths apart simultaneously from the shift register in accordance with an index address, the index address corresponding to the I and Q samples associated with a channel;

performing a parallel sum calculation on the plurality of I and Q samples to produce a partial I and Q result;

accumulating the partial I and Q result with one of a plurality of partial I and Q accumulation results associated with the channel; and

outputting the accumulated I and Q results on channel symbol boundaries corresponding to a spreading factor associated with the channel, the accessing, parallel sum, accumulation, and conditional outputting being performed once per round for each of a plurality of channels.

13. The method of claim 12, wherein the parallel sum calculation comprises:

generating a plurality of I and Q PN sequence values each cycle according to the channel;

despreading the plurality of I and Q samples with the plurality of I and Q PN sequence values to produce a plurality of despread I and Q results; and

summing the plurality of despread I and Q results to produce the partial I and Q result.

14. The method of claim 12, wherein the parallel sum calculation comprises:

generating a plurality of I and Q PN sequence values each cycle according to the channel;

despreading the plurality of I and Q samples with the plurality of I and Q PN sequence values to produce a plurality of despread I and Q results;

generating a plurality of covering sequence values each cycle according to the channel;

decovering the plurality of despread I and Q results with the plurality of covering sequence values to produce a plurality of decovered I and Q results; and

summing the plurality of decovered I and Q results to produce the partial I and Q result.

15. The method of claim 12, wherein the parallel sum calculation comprises:

generating a plurality of I and Q PN sequence values each cycle according to the channel;

despreading the plurality of I and Q samples with the plurality of I and Q PN sequence values to produce a plurality of despread I and Q results;

generating a plurality of phase values each cycle according to the channel;

rotating the plurality of despread results with the plurality of phase values to produce a plurality of rotated I and Q results;

generating a plurality of covering sequence values each cycle according to the channel;

decovering the plurality of rotated I and Q results with the plurality of covering sequence values to produce a plurality of decovered I and Q results; and

summing the plurality of decovered I and Q results to produce the partial I and Q result.

16. The method of claim 12, wherein the parallel sum calculation comprises:

generating a plurality of I and Q PN sequence values each cycle according to the channel;

despreading the plurality of I and Q samples with the plurality of I and Q PN sequence values to produce a plurality of despread I and Q results;

generating a plurality of covering sequence values each cycle according to the channel;

decovering the plurality of despread results with the plurality of covering sequence values to produce a plurality of decovered I and Q results;

summing the plurality of decovered I and Q results to produce an I sum and a Q sum;

generating a phase value each cycle according to the channel; and

rotating the I sum and Q sum with the phase value to produce the partial I and Q result.

17. A finger front end for processing a plurality of channels, comprising:

a shift register for receiving and shifting in I and Q samples, wherein a plurality of the I and Q samples are accessible in parallel fashion in accordance with an index address;

a parallel sum calculator for receiving the plurality of I and Q samples according to the index address and producing an I and Q result;

a scheduler for generating control of the shift register and the parallel sum calculator such that they are time-shared to produce results in sequence for each of the plurality of channels, wherein the control comprises:

an active channel value for indicating which of the plurality of channels corresponds to the output of the parallel sum calculator; and

an index address for accessing the shift register in accordance with the active channel.

18. The finger front end of claim 17, wherein the parallel sum calculator comprises:

a PN generator for generating a plurality of I and Q PN sequence values each cycle according to the active channel;

a plurality of despreaders for despreading the plurality of I and Q samples with the plurality of I and Q PN sequence values to produce a plurality of despread I and Q results; and

a summer for summing the plurality of despread I and Q results to produce the I and Q result.

19. The finger front end of claim 18, wherein the parallel sum calculator further comprises a plurality of rotators for rotating the despread I and Q results according to one or more phase values associated with the active channel and delivering a plurality of rotated I and Q results to the summer for summing to produce the I and Q result.

20. The finger front end of claim 18, wherein the parallel sum calculator further comprises:

a covering sequence generator for producing a plurality of covering sequence values according to the active channel; and

a plurality of decoverers for decovering the despread I and Q results with the plurality of covering sequence values and and delivering a plurality of decovered I and Q results to the summer for summing to produce the I and Q result.

21. The finger front end of claim 19, wherein the parallel sum calculator further comprises:

a covering sequence generator for producing a plurality of covering sequence values according to the active channel; and

a plurality of decoverers for decovering the despread I and Q results with the plurality of covering sequence values and delivering a plurality of decovered I and Q results to the plurality of rotators to produce the plurality of rotated I and Q results.

22. The finger front end of claim 20, wherein the parallel sum calculator further comprises a rotator for rotating the output of the summer with a phase value in accordance with the active channel to produce the I and Q result.

23. The finger front end of claim 17, further comprising an accumulator for accumulating the I and Q result in a partial accumulation for each active channel and conditionally outputting the partial accumulation on symbol boundaries in accordance with the spreading factor associated with the active channel.

24. A finger front end for processing a plurality of channels, parameterized by:

P, a parallelism factor;

S, a sampling rate;

MAX_CHANNELS, the maximum number of channels supported in the plurality of channels, determined by (P*S)-2;

CYCLES_PER_ROUND, the number of cycles in a round, determined by MAX_CHANNELS + 1; and

SHIFTER_LEN, the minimum shift register length, determined by CYCLES_PER_ROUND + (P-1)*S;

comprising:

a shift register of length SHIFTER_LEN for receiving and shifting in I and Q samples at sampling rate S, and wherein a plurality P of the I and Q samples are accessible in parallel fashion in accordance with an index address;

a parallel sum calculator for receiving the P I and Q samples according to the index address and producing an I and Q result;

a scheduler for generating control of the shift register and the parallel sum calculator such that they are time-shared to produce results in sequence for each of the MAX_CHANNELS once per round and wherein the control comprises:

an active channel value for indicating which of the plurality of channels corresponds to the output of the parallel sum calculator; and

an index address for accessing the shift register in accordance with the active channel .

25. The finger front end of claim 24, further comprising an accumulator for accumulating the I and Q result in a partial accumulation for each active channel and conditionally outputting the partial accumulation on symbol boundaries in accordance with the spreading factor associated with the active channel, under control of the scheduler.

26. The finger front end of claim 25, wherein the parallel sum calculator produces, in addition to the I and Q result, partial sums corresponding to spreading factors less than P, and further comprising a selector for selectively outputting the partial accumulation or the partial sums in accordance with the spreading factor associated with the active channel, under control of the scheduler.

27. In a finger front end parameterized by:

P, a parallelism factor;

S, a sampling rate;

MAX_CHANNELS, the maximum number of channels supported in a plurality of channels, determined by (P*S)-2; and

CYCLES_PER_ROUND, the number of cycles in a round, determined by MAX_CHANNELS + 1,

a method for producing an index associated with each channel, index $_{CH}$, for accessing a parallel access shift register, comprising:

in each round of CYCLES_PER_ROUND:

remain idle for one cycle, refrain from accessing the shift register or ignore the results of such access; and

sequence through each channel, one channel per cycle, adjusting each channel's associated index, wherein the index adjustment comprises the following steps:

when the index associated with a channel is less than zero:

increment the index by CYCLES_PER_ROUND;

refrain from accessing the shift register or ignore the results of such access; and

remain idle for the duration of the cycle;

otherwise:

access the shift register utilizing the index;

when a retard command is in effect, decrement the index by 2;

when an advance command is in effect, take no action;

when neither an advance nor retard command is in effect, decrement the index by 1;

regardless of whether an advance or retard command is in effect, increment the index by CYCLES_PER_ROUND - ((P*S) - 1).

28. The method of claim 27, further comprising:

incrementing a PN count value, associated with each channel, by P for each cycle in which the associated index is not less than zero; and

signaling the accumulator to output the partial accumulation on symbol boundaries determined by the spreading factor and PN count value associated with the channel.

29. The method of claim 27, further comprising:

incrementing a PN count value, associated with each channel, by P for each cycle in which the index associated with the channel is not less than zero;

when the spreading factor associated with the channel is P or greater, signaling the accumulator to output the partial accumulation on symbol boundaries determined by the spreading factor and PN count value associated with the channel; and

when the spreading factor associated with the channel is less than P, selecting the partial sums in accordance with the spreading factor.